

REMARKS

Claims 7-13 are pending. Claims 7 and 13 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Entry of this Amendment is respectfully requested since no new issues are raised by the entry of this Amendment and it places the application in condition for allowance or at least in better form for appeal.

Claim Rejections Under 35 U.S.C. § 102 and 103

Claims 7-10 were rejected under 35 U.S.C. § 102(e) over Fang (U.S. Patent No. 6,667,511) and claims 11-13 were rejected under 35 U.S.C. § 103(a) over Fang in view of Sheng et al. (U.S. Patent No. 5,981,404). Applicants respectfully traverse these rejections.

Amended claim 7 recites, in part, a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region that includes sequentially forming an insulating film including an oxide film and a nitride film and a second polysilicon film on the entire structure including the cell region and the peripheral circuit region and patterning the second polysilicon film and the insulating film so that they remain in a given region of said cell region and said peripheral circuit region respectively.

In contrast, Fang discloses that a dielectric layer 322 is formed over the surface of the device and patterned to overlie the poly1 floating gate region. Fang does not disclose that the dielectric layer is formed on peripheral regions 314 and 315 (see, for example, column 10, lines 29-35, and Figures 9f-h). Additionally, since Fang teaches that the dielectric film 322 is not formed over the peripheral regions 314 and 315, Fang does not teach or suggest patterning the second polysilicon film and the insulating film so that they remain in a given region of said cell region and said peripheral circuit region respectively. Fang actually teaches that the dielectric film 322 is only in the region 317, not in the peripheral regions 314, 315. Accordingly, Fang fails to teach, or even suggest, a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region that includes sequentially forming an insulating film including an oxide film and a nitride film and a second polysilicon film on the entire structure including the cell region and the peripheral circuit region and patterning the second polysilicon film and the insulating film so that they remain in a given region of said cell region and said peripheral circuit region respectively, as recited in amended claim 7.

Claim 13 is believed allowable for at least the same reasons presented above with respect to claim 7 since claim 13 recites features similar to the features of claim 7 discussed above.

Claims 8-12 are believed allowable for at least the reasons presented above with respect to claim 7 by virtue of their dependence upon claim 7 and, with respect to claims 11-12, because Sheng does not remedy at least the deficiencies of Fang discussed above with respect to claim 7. Accordingly, Applicants respectfully request reconsideration and withdrawal of these rejections.

Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

MAYER BROWN ROWE & MAW LLP

By: 

Yoon S. Ham
Registration No. 45,307
Direct No. (202) 263-3280

YSH/VVK

Intellectual Property Group
1909 K Street, N.W.
Washington, D.C. 20006-1101
(202) 263-3000 Telephone
(202) 263-3300 Facsimile

Date: October 21, 2005